DESIGN RAM MEMORIES BY USING FLIP-FLOP CIRCUITS

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ABSTRACT

Memories are considered essential parts in computer system and the main component of storage system of data ,during the operation time , which leads to accomplish the required commands , so the designing of RAM is regarded the most important because of its vital role in operation speed the microprocessor performs , therefore Flip – Flop Circuits are used to design RAM by representing each bit with a Flip – Flop on to be connected with the microprocessor in order to organize their bite addresses . There are several types of Flip-Flop circuits such as SR , JK , D and Master slave , however the preferable ones is Flip–Flop D.

Keywords: Flip – Flop, SR, D, CS, RW, Decoder, ADRS, BC, RAM, SRAM, DRAM.

1. INTRODUCTION

As it is called in the main computer's cache because it is a place of temporary work in the computer in which the programs are loaded operating and doing implementation.The computer's memory consists of electronic integrated circuits Chips ultra-fine. The bank, which information is stored in it while you work on your computer. The unit of measurement is megabytes this memory Mb.Whenever he was in the computer's memory, "RAM" size is greater, the performance will be better. Where the computer is characterized by containing the largest that hecan deal with modern memory programs and these programs are often of great size and require large memory before you do the work properly.

There are programs and files you actually need a huge volume of private memory if you also editing operations, such as working in the editing large images or extended thread Spreadsheets complex. The presence of large memory allows you to work on multiple programs at the same time and in a manner unusual. Thus, the possible move from one program to another instantaneously, depending on the tasks that are to deal with it in the computer. This is better than that you close the program in which they operate to open another program. It is also features a large memory in the computer is that they help make faster computer at work, and is characterized by internal computer design the possibility of increasing or adding new memory to him easily and quickly.

Easy to understand how to increase the memory size makes the computer able to do with the circulation of larger size files, or run multiple programs at the same time,but how are the larger memories by making the fastest computer at work? The answer to this is that the larger memory reduces the need for the Windows operating program that the use of a large area of the disk to temporarily turning it as an extension of memory. These new memory on the hard disk is very much slower than real memory. If the original memory in the computer were not enough to work the Windows program starts to work slowly but with real memory and converts some of what is written in the memory to the hard drive so that it frees up some memory temporarily. In the case of the need for the memory of those transferred to the hard drive and Windows it is re-converted to a second memory to be used. This work gives the perception that the computer has more memory than is the reality. And also it makes computer sometimes

able to perform the functions even if you do not have enough computer memory.[1]

This work is good on one hand but on the other hand, of the disadvantages is that "read" the memory and "writing" any review process information and registration, which is made on the hard disk (virtual memory) is a very slow process compared to what is on the main memory. Therefore he whenever the size of memory in the largest computer whenever the computer is faster.

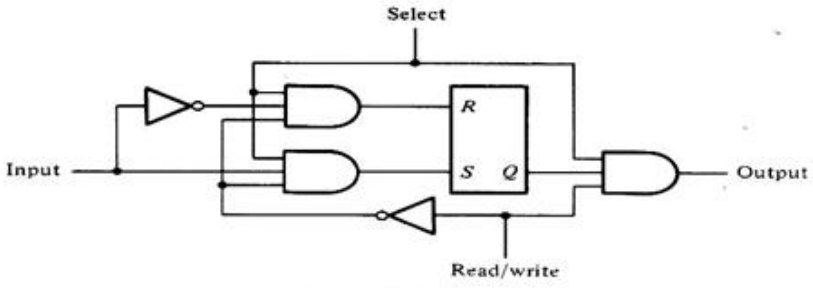
RAM memories can be classified according to the installation of internal storage where cell into two types:

1. Static RAM memory (SRAM) Static RAM: high cost, relatively high speed.

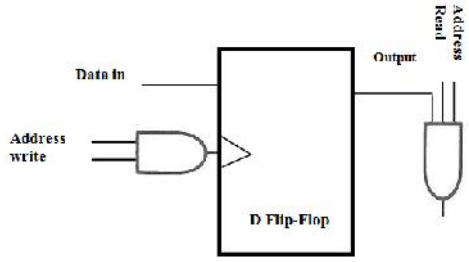
2. Dynamic RAM memory (DRAM) Dynamic RAM. [2]

2. INTERNAL CONSTRUCTION

The internal construction of a random-access memory of m words with n bits per word consists of m*n binary storage calls and associated decoding circuits for selecting individual words. The binary storage cell is the basic building block of a memory unit.The equivalent logic of a binary cell that stores one bit of information is shown fig (1). Although the cell is shown to include gates and Flip-Flop, internally, it is constructed with two transistors having multiple inputs. A binary storage cell must be very small in order to be able to pack as many cells as possible in the area available in the integrated-circuit chip. [4] ,[3]

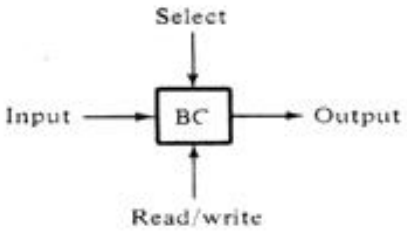


(SR Flip-Flop)



(D Flip-Flop)

(a) Logic diagram



(b) Block diagram

Fig.1 Memory Cell

3. MEMORY DESIGN USING FLIP-FLOP:

The Memory design is simple, you should know that the memory is a set of cells, each cell contains a set of bits called words. A memory word is a group of 1's and 0's and may represent a number; A group of eight bits is

called a byte. so when the memory industry, the basic unit of design is the design of each word of these words memory, has been the use of Flip_Flop as each word is represented by Flip-Flop .

The binary cell stores one bit in its internal flip-flop. It has three inputs and one output. The select input enables the cell for reading or writing and the read/write input determines the cell operation when it is selected. A 1 in the read/write input providers the read operation by forming a path from the flip-flop to the output terminal. A 0 in the read/write input providers the write operation by forming a path from the input terminal to the flip-flop. Note that the flip-flop operates without a clock and is similar to an SR latch.

The logical construction of RAM consist of n words of n bits each and has a total of n*n binary cells. Each block labeled BC represents the binary cell with three inputs and one output, as specified in fig. (1-b). A memory with n words needs n/ln2

Word number= $2^{\text{address lines number}}$

The m address inputs go through a m*n decoder to select one of the n words. The decoder is enabled with the memory-enable input. When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected. With the memory enable at 1, one of the n words is selected, dictated by the value in the m address lines. Once a word has been selected, the read/write input determines the operation. During the read operation, the n bits of the selected word go through OR gates to the output terminals. During the write operation, the data available in the lines are transferred into the n binary cells of the selected word. The binary cells that are not selected are disabled and their previous binary values remain unchanged. When the memory-enable input that goes into the decoder to 0,

none of the words are selected and the contents of all cells remain unchanged regardless of the value of the read/write input.

For example, the logical construction of a small RAM is shown fig. (2). It consists of 4 words of 3 bits each and has a total of 12 binary cells. A memory with four words needs two address lines. The two address inputs go through a 2*4 decoder to select one of the four words.

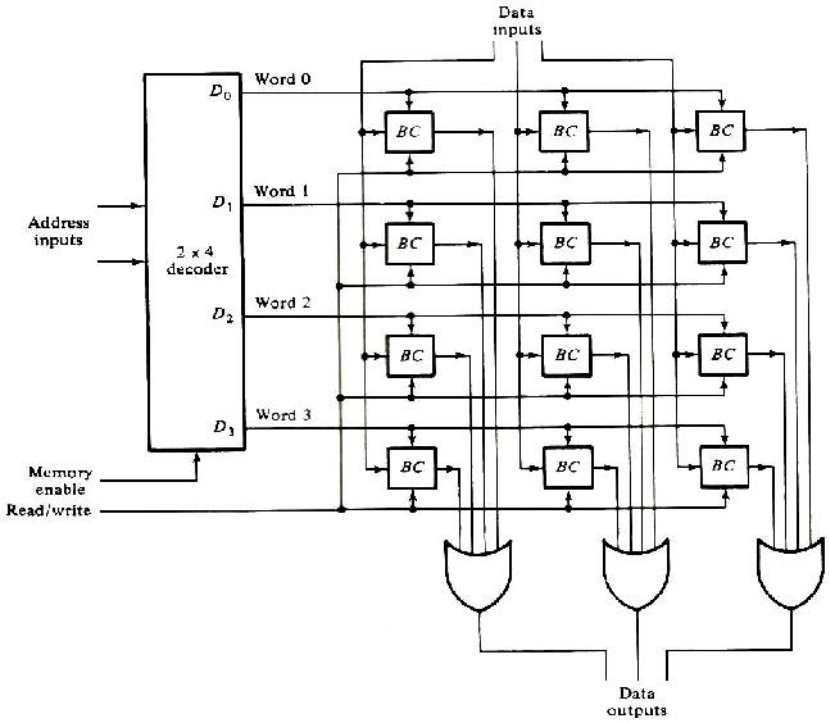


Fig.2 Logical construction of a 4 * 3 RAMS

Commercial random-access memories may have a capacity of thousands of words and each word may range from. The logical construction of a large capacity memory would be a direct extension of the configuration shown here. A memory with 2^k words of n bits per word requires k address lines

that go into a $k*2^k$ decoder. Each one of the decoder outputs selects one word of n bits for reading or writing.

4. ARRAY OF RAM CHIPS

Integrated-circuit RAM chips are available in a variety of size. If the memory unit needed for an application is larger than the capacity of one chip, it is necessary to combine a number of chips in an array to from the required memory size. The capacity of the memory depends on two parameters: the number of word and the number of bits per word. An increase in the number of words requires that we increase the address length. Every bit added to the length of address doubles the number of words in memory. The increase in the number of bits per word requires that we increase the length of the data input and output lines, but the address length remains the same.

To demonstrate with an example, let us first introduce a typical RAM chip, as shown in fig (3). The capacity of the RAM is 1024 words of 8 bits each. It requires a 10 bit address and 8 input and output lines. These are shown in the block diagram by a single line and a number indicating the total number of inputs or outputs.

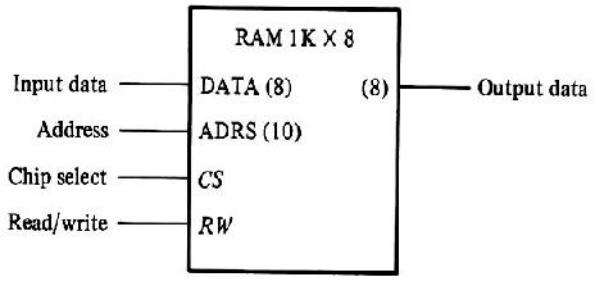


Fig.3 Block diagram of a 1K * 8 RAM chip

The chip select (CS) input selects the particular RAM chip and the read/write (RW) input specifies the read or write operation when the chip is selected.

Suppose that we want to increase the number of word in the memory by using two or more RAM chips. Since every bit added to the address doubles the binary number that can be formed, it is natural to increase the number of words in factors of two. For example, two RAM chips will double the number of words and add one bit to the composite address. Four RAM chips multiply the number of words by 4 and add two bits to the composite address.

Consider the possibility of constructing a 4K*8 RAM with four 1k*8 RAM chips. This is shown in fig (4). The 8 input data lines go to all the chips. The outputs must be OR together to from the common 8 output data lines. (The OR gates are not shown in the diagram). The 4K word memory requires a 12- bit address. The 10 least significant bits of the address are applied to the address input of all four chips.The other two most significant bits are applied to a 2*4 decoder. The four outputs of the decoder are applied to the CS inputs of each chip. The memory is disabled when the memory-enable input of the decoder is equal to 0. This causes all four outputs of the decoder to be in the 0 state and none of the chips are selected. When the decoder is enabled, address bits 12 and 11 determine the particular chip that is selected. If bits 12 and 11 are equal to 00, the first RAM chip is selected. The remaining ten address bits select a word within the chip in the range from 0 to 1023. The next 1024 words are selected from the second RAM chip with a 12-bit address that starts with 01 and follows by the ten bits from the

common address lines. The address range for each chip is listed in decimal over its block diagram in Fig. (4).

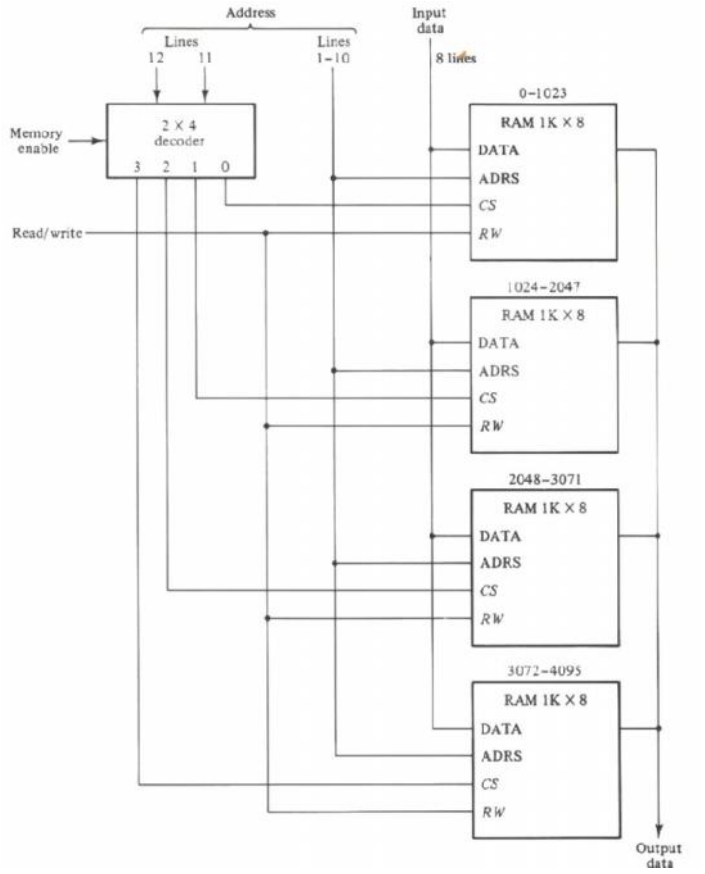


Fig.4 Block diagram of a 4K * 8 RAM

It is also possible to combine two chips to from a composite memory containing the same number of word but with twice as many bits in each word. Figure (5) shows the interconnection of two 1K*8 chips to from a 1K*16 memory. The 16 input and output data lines are split between the two chips. Both receive the same 10-bit address and the common CS and RW control inputs.

The two techniques just described may be combined to assemble an array of identical chips into a large-capacity memory. The composite memory will have a number of bits per word that is a multiple of that for one chip.

The total number of words will increase in factors of 2 times the word capacity of one chip. An external decoder is needed to select the individual chips from the additional address bits of the composite memory.

To reduce the number of pins in the package, many RAM integrated circuits provide common terminals for the input data and output data. The common terminals are said to be bidirectional, which means that for the read operation, they act as outputs, and for the write operation, they act as input[4].

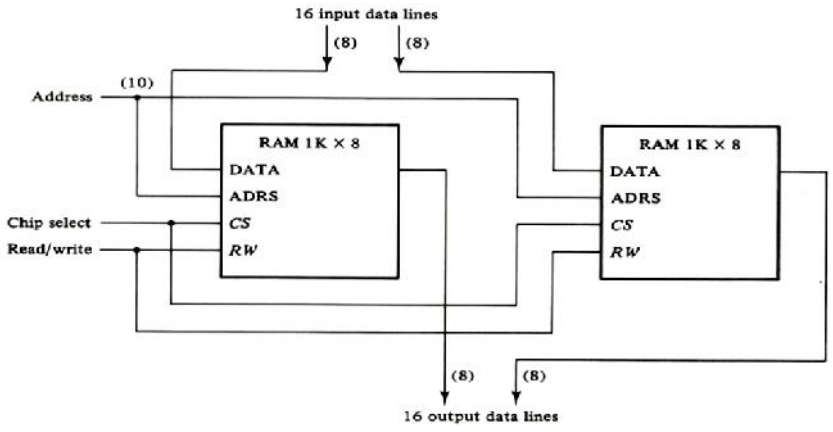


Fig.5 Block diagram of a 1K*16 RAM

5. CONCLUSION

We have noticed clearly that all memory cells are separate from each other and independent in their work therefore been linked to these cells gates logical OR, a gateway linking every bit in a cell to another bit in another cell and so that is linked to all cells.The Memory RAM industry has a very great

importance to the RAM memory of importance in the computer system so take them in this paper and explain designed using Flip_Flop gates because of its ease and simplicity in understanding and design instead of using the complex transistor in design mode, because when the memory is designed using transistor must to have a great knowledge of his way.But in general, this easy-to-Memory and industry must take into account the possibility of its industry locally.

Finally we have found that the best Flip_ Flop can be used in the design of memories is Flip_Flop D.

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